

# Envelope Amplifier for RF Amplifier based on Multilevel Converter

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**Abstract-** Modern transmitters usually have to amplify and transmit signals with simultaneous envelope and phase modulation. Due to this property of the transmitted signal, linear power amplifiers (class A, B or AB) are usually used as a solution for the power amplifier stage. These amplifiers have high linearity, but suffer from low efficiency when the transmitted signal has low peak-to-average power ratio. The Kahn envelope elimination and restoration (EER) technique is used to enhance efficiency of RF transmitters, by combining highly efficient, nonlinear RF amplifier (class D or E) with a highly efficient envelope amplifier in order to obtain linear and highly efficient RF amplifier. This paper presents a solution for the envelope amplifier based on a combination of multilevel converter and linear regulator. The proposed solution can reproduce any signal with maximal spectral component of 2 MHz and give instantaneous maximal power of 50 W. The efficiency measurements show that when the signals with low average value are transmitted, it has up to 15% higher efficiency than linear regulator that is used as a conventional solution. Additionally, the algorithm for selection of voltage levels for the multilevel converter is explained, as well.

## I. INTRODUCTION

In the modern world of today, the demand for broadband and wireless services is growing on a daily basis. One of direct consequences of this growth is certainly the growth of the networks that have to provide these services and the problem is their energy consumption. Some estimations showed that a 1% of planet's global energy consumption in 2007 was made by telecommunication industry [1]. In [2] is explained that the efficiency of the first generation 3G radio base stations is just few percents, and that the efficiency of the employed power amplifiers is just 6%. The impact of power amplifier's efficiency can be seen in the information that if the power amplifiers could improve its efficiency by 10% the overall efficiency would be raised by 6%. Therefore, the questions are rising. Why do the power amplifiers have low efficiency? Is there a possibility to increase it?

The transmitters usually employ digital modulations such as QPSK combined with spread spectrum techniques like CDMA or WCDMA. The modulated signals are later amplified by using highly linear, but low efficient linear amplifiers like class A or class B amplifiers. In the ideal case, the maximal efficiency for class A and class B amplifiers reaches 50% and 78.5% respectively. However, the theoretical value is usually reduced by the factor of 0.8 to 0.85 due to various losses [3]. Additionally, the maximal efficiency is calculated in the case of the signal that has constant amplitude. The signals that are amplified by the PA and latter transmitted usually have time varying envelope, so that the only way to calculate the efficiency of the PA is to use the

probability density function [4]. The probability density function of the envelope gives the relative amount of time a signal spends at various amplitudes, Figure 1 [4]. Frequency modulated signals or constant wave signals have constant envelope and, therefore, linear power amplifiers or class E amplifiers could be optimal solution for the transmitter's PA. On the other hand, noise and multiple carriers have Rayleigh-distributed envelope and high peak-to-average power ratio (PAPR) [3]. Instantaneous efficiency is the efficiency of the PA at one certain output level.

The instantaneous efficiency of class A and class B amplifier in the case of various sine wave amplitudes is shown in Figure 2. From figures 1 and 2 it can be seen that the signals with high PAPR have the highest probability in the zone where linear amplifiers have very low efficiency (approximately 15% for class B) and that is the main reason for low efficiency of these PA applied in RF systems.

The Kahn envelope elimination and restoration (EER) technique is used to enhance efficiency of RF transmitter. Figure 3 shows block diagram of one EER transmitter. This technique combines a highly efficient, but nonlinear RF PA (class D or class E for example) with a highly efficient envelope amplifier to implement high-efficiency linear RF PA [5].

The basis for EER is the equivalence of any narrowband signal to simultaneous amplitude (envelope) and phase modulation:

$$V_{RF}(t) = I(t) \cos(2\pi ft) - Q(t) \sin(2\pi ft) = A(t) \cos(2\pi ft + \theta(t)) \quad (1)$$

$$\theta(t) = \arctg\left(\frac{Q(t)}{I(t)}\right) \quad A(t) = \sqrt{I(t)^2 + Q(t)^2} \quad (2)$$

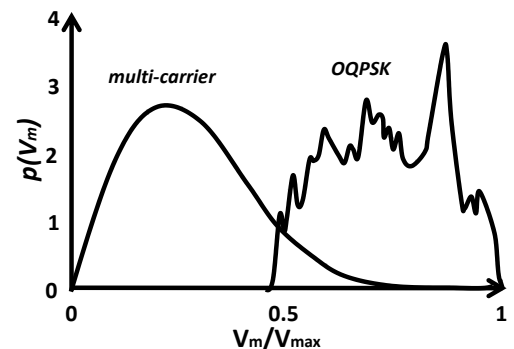


Figure 1. Probability density function of the signal's envelope for different modulation techniques

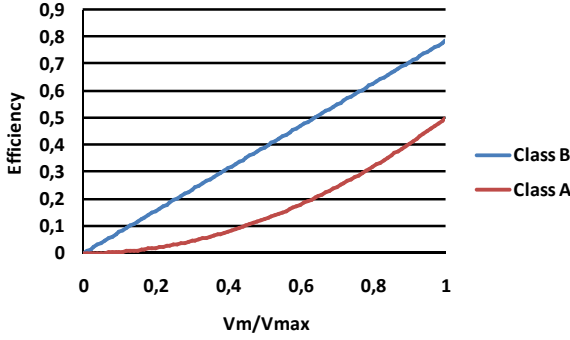


Figure 2. Instantaneous efficiency of class A and class B amplifier in the case of various sine wave amplitudes

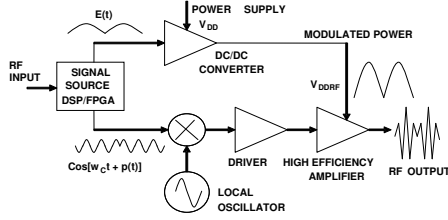


Figure 3. Block Scheme of Kahn-technique Transmitter

where  $f$  is the carrier frequency,  $Q(t)$  and  $I(t)$  are modulated signals.

Therefore, analyzing the equation (1), it can be concluded that the nonlinear RF PA should be used to change the phase of transmitted signal, and the envelope amplifier to apply amplitude modulation. By applying this technique it is possible to achieve 3 to 5 times better efficiency comparing with standard class A and class B amplifiers [3,4, 6, 7].

The envelope amplifier should have fast dynamic response, high efficiency and minimal interference with the output spectrum of the transmitter. In the state of the art, several solutions for the envelope amplifier can be found, such as a simple buck converter (class S modulator) in [8, 9], multiphase buck converter in [10], three-level converter in [11] or linear assisted switching amplifier [12, 13]. These solutions do not exceed the bandwidth of few hundred kHz and the output power is from the range of mW up to several tens of watts [4]. In [14, 15] buck converter is integrated and the switching frequency is in range of several MHz, but with small output power, in the range of mW.

The envelope amplifier needs to have high efficiency, and therefore, a dc-dc converter would be a first idea for the solution. Nevertheless, in order to provide high bandwidth that is necessary to follow the envelope reference, these converters have to use switching frequency up to five times higher than the requested bandwidth (for the bandwidth of 1 MHz it would be necessary to apply switching frequency of, at least, 5 MHz) [16]. The efficiency of dc-dc converters drops heavily when the switching frequency is increased; therefore, the efficiency of whole system drops as well. The second problem is the output filter of the converter, because its design can be very complicated due to very strict restrictions regarding the voltage ripple and spectral interference. In some papers, it is proposed to use double LC filter [8], but the use of this filter could decrease the maximum bandwidth.

The solution presented in this paper does not need complicated filter design and it is not necessary to apply very high switching

frequency in order to obtain the bandwidth of several MHz. The presented system can reproduce a sine wave or any other reference with maximal spectral component of 2 MHz, and give the instantaneous maximal power of 50 W.

## II. PROPOSED TOPOLOGY

The proposed topology consists of a multilevel converter in series with a high slew rate linear regulator. The main idea of the solution can be seen in Figure 4. The multilevel converter has to supply the linear regulator and it has to provide discrete voltage levels that are as close as possible to the output voltage of the envelope amplifier. If this is fulfilled, the power losses on the linear regulator will be minimal, because they are directly proportional to the difference of its input and output voltage. However, in order to guarantee correct work of the linear regulator, the output voltage of the multilevel converter always has to be higher than the output voltage of the linear regulator.

The linear regulator can be designed to have very high bandwidth, and it should filter all the noise that could come from the multilevel converter. Therefore, the multilevel converter does not need any filter at its output and the design of the complicated filter as in the case of switched converters is avoided.

There are several possibilities to implement the multilevel converter for this application, and some of them are presented in [17].

In the prototype that is implemented in this paper, the solution for the multilevel converter is based on several two-level voltage cells that are put in series, Figure 5. Therefore, the output of this converter can be represented as:

$$v_o = \sum_{i=1}^N a_i V_i \quad (3)$$

where, the  $N$  is the total number of the implemented cells,  $a_i$  takes the value of 0 when the  $i^{th}$  cell is turned off and 1 when it is turned on and  $V_i$  is the supply voltage of the  $i^{th}$  cell.

Although there are multilevel solutions with only one input voltage, this one is different and it has to be supplied by several voltages. The reason lies in the fact that the reference signal does not have to be symmetric, like it is in the case when multilevel converters are used for inverter applications. The implemented design guarantees that each cell will have its supply voltage all the time, regardless on the reference signal sent to the envelope amplifier.

Due to the independent voltages that have to be produced, it is obvious that it is required to introduce a single-input multiple-outputs stage that will generate all the needed voltages. In the case of the first multilevel solution, the output voltages are the voltage levels that are needed in the system, and they are all referenced to the ground. When the multilevel converter is implemented with two-level and three-level cells, the output voltages should be isolated and referenced to the different grounds. The cell's input voltage does not need to be regulated accurately, because the fine regulation will be done by the linear regulator that is connected in series with the multilevel converter. Additionally, in the case of three-level cell, the cell's input source has to be bidirectional, because, depending on the state of the switches, the source will sink or source the current to the load.

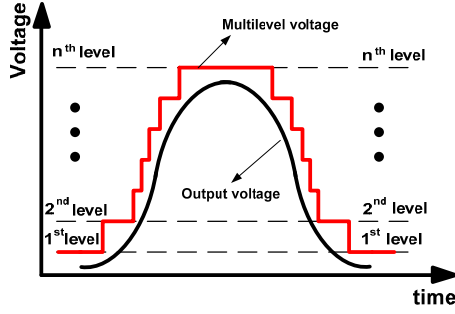


Figure 4. Time diagrams of the proposed envelope amplifier

The envelope amplifier that has been prototyped consists of: (i) a high slew rate linear regulator, (ii) a multilevel converter with two-level cells and (iii) a single-input multiple-outputs, isolated dc-dc converter (multiple-outputs flyback converter) that provides dc voltages to the cells of multilevel converter, Figure 6.

The implemented multilevel converter is composed of several two level cells that are placed in series, and each cell can be turned on or off independently.

The class E amplifier that is used for transmitter's phase modulation is supplied by the envelope amplifier and it behaves as a resistive load, approximately 12  $\Omega$ .

The advantage of this topology is that it provides high dynamics of the output voltage with increased efficiency comparing with linear regulator that is supplied with constant voltage and that its control is very simple and robust. The drawback is that each stage of the system (multiple-output converter, multilevel converter and linear regulator) needs to have very high efficiency, because the total efficiency is the product of individual efficiencies. However, it is still possible to achieve high overall efficiency, as it will be seen later.

### III. CONTROL OF ENVELOPE AMPLIFIER

The first stage, single-input multiple-outputs converter, is controlled by a voltage feedback from one of its output, because all the other outputs will follow the controlled one. The bandwidth of this stage does not have to be high; therefore, the switching frequency of the multiple-outputs flyback can be very low in order to increase its efficiency.

The reference signal that should be reproduced is sent to the multilevel through the block named "triggering logic" that consists of simple comparator logic. The each cell is turned on when the reference signal is higher than a certain value (which is different for each cell), Figure 8. Consequently, the output of the multilevel converter will have discrete levels (depending on the number of implemented cells) and each cell inside the multilevel converter will switch at the maximum frequency of the reference signal, i.e. the frequency of the requested bandwidth. Even more, the dynamic response of the multilevel converter will depend only on the speed of the MOSFETs that are used inside the cells.

The same reference signal enters in the second stage and in the linear regulator (post regulator). The linear regulator reference has to be synchronized with the output voltage of the multilevel converter in order to guarantee that the system's output voltage (between points C and D, Figure 6) will be always lower than the output voltage of the multilevel converter (points A and B, Figure 6) and, therefore, correctly reproduced. Due to the finite time to turn MOSFETs on and off, the output of the multilevel converter

is delayed comparing it with the envelope reference, therefore, a delay filter which will compensate this delay is introduced between the reference signal and the linear regulator.

In order to achieve high bandwidth of the linear regulator, it is necessary to use a high bandwidth operational amplifier in the feedback loop and to use a MOSFET with low parasitic capacitance between its gate and source as a pass element of the linear regulator.

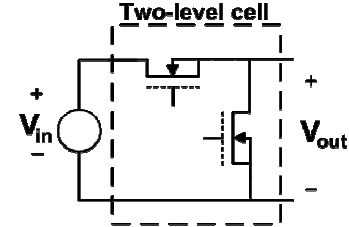


Figure 5. Voltage cell that is used as the solution to implement a multilevel converter

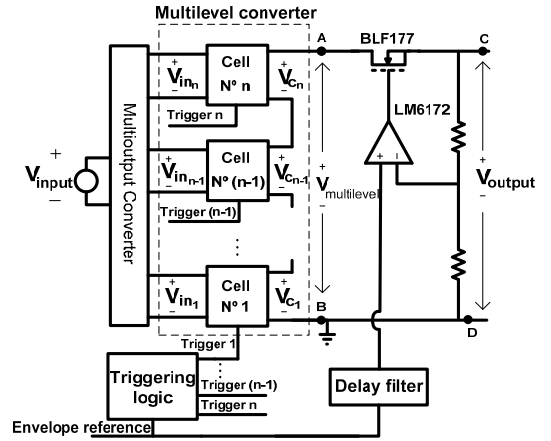


Figure 6. Block diagram of the implemented envelope amplifier

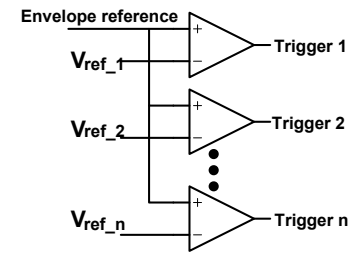


Figure 7. Comparator logic that is used to control on/off states for each cell of the multilevel converter

### IV. EFFICIENCY CONSIDERATIONS

#### A. First stage

In order to obtain high overall efficiency it is necessary to maximize the efficiency of each system stage. As a simple and robust solution for the isolated multiple-outputs dc-dc converter a flyback with multiple-outputs has been selected. However, although this is very simple solution, it is not the optimal one, looking from the point of efficiency. Due to voltage fall on the secondary side diode the efficiency cannot be higher than  $V_{cell}/(V_{cell}+V_{diode})$  (in the case when all the outputs have the same voltage). A solution that provides isolated outputs and uses synchronous rectification on the secondary side could have better efficiency. Additionally, if a single transformer is used for all the

outputs its construction is another problem, especially if the high number of cells is implemented. It is necessary to optimize its design having in mind the gap and proximity effect that could increase the transformer losses. In order to minimize the losses due to the leakage inductance of the transformer, active clamping is applied.

#### B. Second stage

The losses in the multilevel converter are due to MOSFET's conduction and switching. The conduction losses will depend only on the MOSFET selection, while the switching losses will depend on the MOSFET's characteristics and supply voltage of the multilevel cell. The concept of multilevel converter enables the usage of low voltages in each cell, and therefore, there should be relatively low switching losses. However, the higher number of multilevel cells is, the higher conduction losses are, and consequently, there is a tradeoff, between the conduction and switching losses that must be taken into account.

#### C. Third stage

The linear regulator is supplied by the multilevel converter, and, depending on the current voltage level on its input and output, its efficiency will vary. Assuming that the transmitted signal use CDMA technique and that the envelope would have probability density distribution like in [18], it is possible to optimize the multilevel cell's voltage and the number of levels. By optimizing the levels of the multilevel converter, the efficiency can be increased 5% to 6% comparing with the multilevel with equidistant voltage levels, Table 1. Figure 8 shows the instantaneous efficiency of the linear regulator for different number of levels and different selection of voltage levels.

### V. DESIGNED SYSTEM

In order to prove the concept two prototypes of envelope amplifier have been made. The specifications for both prototypes are as follows:

- Variable output voltage from 0 V to 23 V
- The maximum instantaneous power is 50 W
- The maximum frequency of the reference signal is 2 MHz

#### A. First prototype

The first envelope amplifier prototype consists of:

- single-input multiple-outputs flyback (first stage)
  - Input voltage is 24 V
  - Five 6 V outputs
  - Switching frequency is 50 kHz
  - The maximum instantaneous power is, approximately, 50 W
- multilevel converter with five two-level cells (second stage)
- linear regulator (post regulator).
  - MOSFET BLF177 as the pass element
  - Operational amplifier LM6172 for the feedback

During the tests with the first prototype some bigger problems were discovered. The prototype had problems with noise and parasitic elements of the PCB. These problems led to distortion of the output signal. The higher frequency of the output signal, the problem was more evident, Figures 9 and 10.

The efficiency of the multiple-outputs flyback converter caused some problems as well. The transformer had five secondary outputs, and it was very difficult to build it. Even more, once it was build, the losses were very high, mostly because of the proximity and gap effect.

TABLE I

THEORETICAL EFFICIENCY OF THE LINER REGULATOR IN A CASE WHEN IT IS SUPPLIED WITH A MULTILEVEL CONVERTER WITH OPTIMIZED AND EQUIDISTANT VOLTAGE LEVELS

Number of cells	Optimized cell's voltage (Scaled with the $V_{outmax}$ )	Efficiency of the ideal linear regulator with optimized voltage levels	Efficiency of the ideal linear regulator with equidistant voltage levels
1	1	51.8%	51.8%
2	1, 0.62	72.5%	68.1%
3	1, 0.71, 0.51	81.1%	75.4%
4	1, 0.71, 0.57, 0.42	85.9%	80.7%

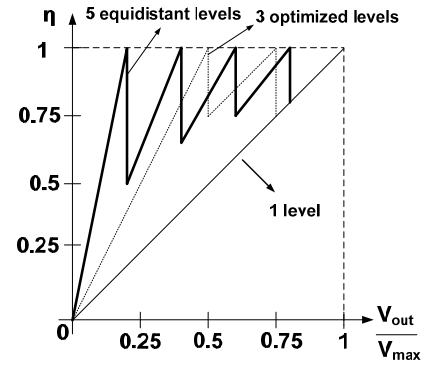


Figure 8. Theoretical efficiency of the used linear regulator when it is supplied with constant voltage and proposed multilevel converter

It was clear that the design needed optimization and better layout. By using Ansoft Quic3D the parasitic components were extracted and one of the alarming conclusions was that by implementing high number of cells the parasitic inductance that was distributed on the current path through the multilevel converter was getting bigger, and at high frequencies it was limiting the converter's dynamics. Therefore, it was necessary to optimize the number of levels as well.

#### B. Second prototype

The second prototype's specifications are as follows:

- single-input multiple-outputs flyback (first stage)
  - Input voltage is 24 V
  - Two 6 V outputs and one 12 V output
  - Switching frequency is 50 kHz
  - The maximum instantaneous power is, approximately, 50 W
- multilevel converter with two two-level cells (second stage)
- linear regulator (post regulator).
  - MOSFET BLF177 as the pass element
  - Operational amplifier LM6172 for the feedback

Once, when the number of levels was determined, the optimization of flyback's transformer was done. In order to solve the problem of gap and proximity effect, we used PExprt.

The prototype's layout was optimized using Q3D Extractor. Q3D Extractor is a tool that extracts parasitic components of the given layout using the method of Partial Element Equivalent

Circuit (PEEC). The result that is obtained is an equivalent circuit that can be simulated in CAD tools as SPICE. This possibility is the main advantage of this method over Finite Element Method (FEM). If the FEM had been applied, the result would have been the distribution of electric and magnetic field and that is the information that is hardly useful in order to optimize the prototype's layout. The process of the layout optimization is shown in Figure 11. It is an iterative process that is composed of making the layout, extracting its electric model, simulating complete system (the system components and the system layout) and if the results are not good enough repeating the same cycles until the desired response is obtained. Figure 12 shows a comparison between multilevel output voltage obtained by simulation using information from Q3D Extractor and voltage obtained by a measurement on the prototype. As it can be seen there is great similarity between these two traces.

In Figure 13 pictures of the enhanced and optimized prototype are shown.

Figure 14 shows the multilevel and system's output voltage in the case of 500 kHz and 2 MHz sine wave. In these figures it can be seen that the noise problem was resolved. The output voltages are much clearer, however, whenever the multilevel converter changes its output voltage there is small glitch in the output voltage. The reason is the finite bandwidth of the linear regulator. Step changes of the multilevel's voltage are composed of very high harmonics that are higher than the regulator's bandwidth. Therefore, the linear regulator is not able to react and stabilize the output voltage very well in these moments. In order to make these transitions "softer", with less high spectral components, the resistance in the gates of MOSFET that form the multilevel converter is increased. In this way, the MOSFET's transition time is increased, and therefore the switching loss as well, but, the linear regulator can react better and the glitch in the output voltage is almost removed.

The multilevel solution has better efficiency than linear regulator when signals with small average value are transmitted, and that is mostly the case when the EER technique is applied. The efficiency of the envelope amplifier is constant (around 43%) when small signals are reproduced, the reason is that only the 12V cell is active, and there is not any switching losses, only conduction losses, regardless on the frequency of the sine wave. The efficiency of the system is measured for different sine waves and the results are summarized in Table 2.

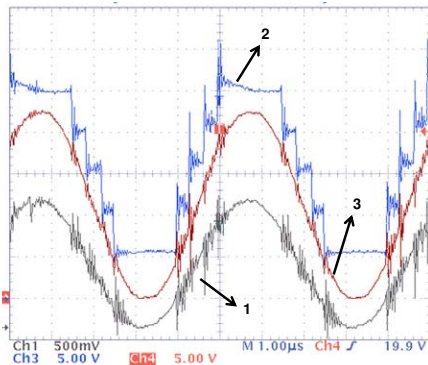


Figure 9. Waveforms of reference signal at 200kHz (label 1), multilevel (label 2) and output voltage (label 3)

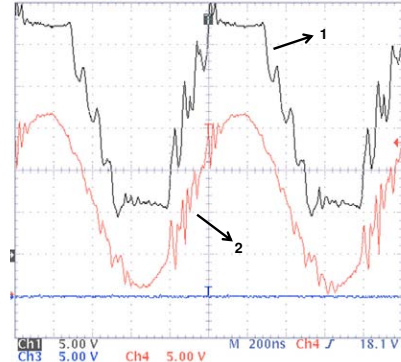


Figure 10. Waveforms of multilevel (label 1) and output voltage (label 2) at 1MHz

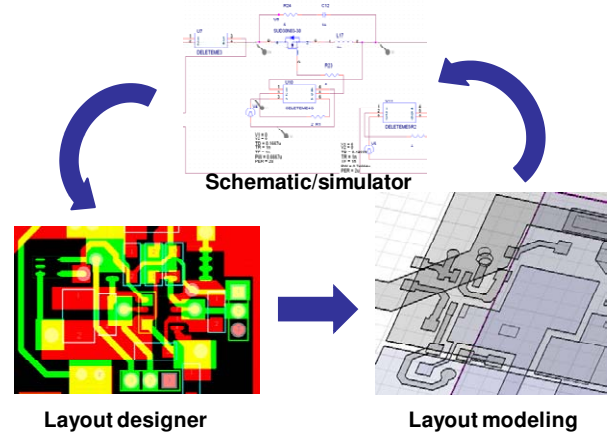


Figure 11. The iterative process of the layout optimization

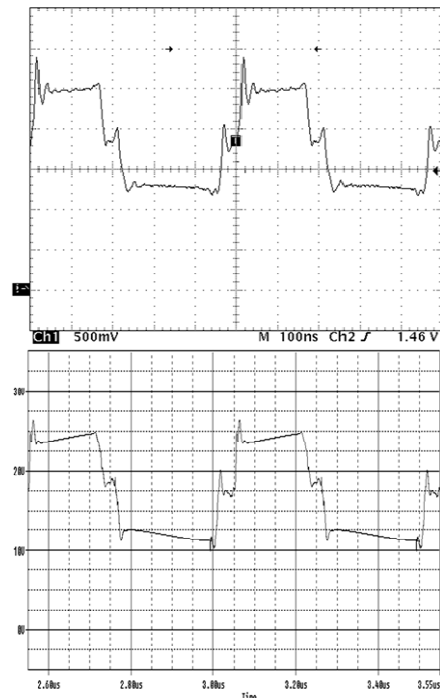


Figure 12. Comparison of the measured output voltage of the multilevel converter (above) and simulated multilevel's output voltage (below)

## VI. CONCLUSIONS

In this paper a novel solution for power supply for EER technique is presented. The solution is composed of a multilevel converter that is put in series with a linear regulator. Several solutions for the multilevel converter are proposed. This



architecture provides high bandwidth of the system (2 MHz) and small influence on adjacent communication channels. The number of levels is optimized having in mind the tradeoff between the feasibility of the multilevel converter (due to parasitic components on the PCB) and the increased efficiency of the linear regulator. The system's efficiency has been measured for the various 2 MHz and 0.5 kHz sine waves. When the sine wave has small average value (what is usually the case in the case of RF amplifier) the proposed system has better efficiency up to 15% than linear regulator.

TABLE II

MEASURED EFFICIENCY OF THE IMPLEMENTED ENVELOPE AMPLIFIER FOR DIFFERENT SINE WAVES COMPARED WITH THE THEORETICAL EFFICIENCY OF AN IDEAL LINEAR REGULATOR SUPPLIED BY 23 V

$V_{sin}(V)$	Sine wave frequency (MHz)	Measured efficiency of the flyback converter	Measured efficiency of the envelope amplifier	Theoretical efficiency of an ideal linear regulator supplied by 23V
0-9	2	94%	43.7%	29.3%
5-14	2	93%	58.8%	45.9%
0-22.5	2	91%	68.3%	73.4%
0-9	0.5	91%	43.3%	29.3%
5-14	0.5	91%	58.9%	45.9%
0-22.5	0.5	94%	69.7%	73.4%

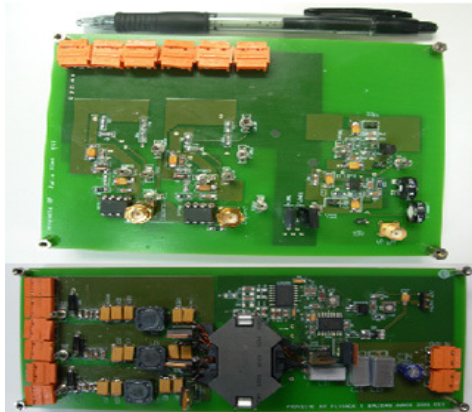


Figure 13. Photograph of implemented multilevel converter

#### REFERENCES

- [1] S.Roy, "Energy Logic for Telecommunications", white paper for Emerson Network Power, September 2008
- [2] G.Pierre, "Power System Efficiency in Wireless Communication", Applied Power Electronics Conference, APEC '06, special presentations
- [3] F.H. Raab, D.J. Rupp, "High efficiency single sideband HF/VHF transmitter based upon envelope elimination and restoration", Sixth Intern. Conference on HF Radio Systems and Techniques, 4-7 July, 1994, Pages:21-25
- [4] F.H. Raab, B.E.Sigmon, R.G.Myers, R.M. Jackson, "L-Band Transmitter Using Kahn EER Technique", Transactions on Microwave Theories and Techniques, Volume 46, Issue 12, Part 2, Pages: 2220-2225, December 1998.
- [5] F.H. Raab, P. Asbeck, S. Cripps, P.B. Kenington, Z.B. Popovic, N. Potheary, J.F. Sevic, N.O. Sokal, "Power Amplifiers and Transmitters for RF and Microwave"
- [6] A.A.M. Saleh, D.C. Cox, "Improving the Power Added Efficiency of FET Amplifiers Operating with Varying-Envelope Signals", Trans. on Microwave Theories and Techniques, vol. MTT-31, no.1, pp.51-56, Jan.1983.
- [7] F.H. Raab, "Efficiency of Envelope-tracking RF Power Amplifier Systems", Proc.. RF Expo East'86, pp. 303-311.
- [8] P. Midya, K. Haddad, L. Connell, S. Bergstedt, B. Roegner, "Tracking power converter for supply modulation of RF power amplifiers," IEEE Power Electronics Specialists Conference, PESC. 2001, Vol. 3, Pages:1540 – 1545
- [9] J. Staudinger, B. Gilsdorf, D. Newman, G. Norris, G. Sadowiczak, R. Sherman, T. Quach, "High efficiency CDMA RF power amplifier using dynamic envelope tracking technique," Microwave Symposium Digest, IEEE MTT-S International, Vol. 2, June 2000, Pages: 873-876
- [10] A. Soto, J.A. Oliver, J.A. Cobos, J. Cezon, F. Arevalo, "Power supply for a radio transmitter with modulated supply voltage", Applied Power Electronics Conference, APEC '04, Volume: 1, Feb. 2004 Pages:392 – 398
- [11] V. Yousefzadeh, E. Alarcon, D. Maksimovic, "Three-level buck converter for envelope tracking in RF power amplifiers," IEEE Trans. on Power Electronics, Volume:21, Issue: 2, March 2006, Pages:549 – 552
- [12] US Patent No. 6084468, Method and Apparatus for High Efficiency Wideband Power Amplification, July 2000.
- [13] V. Yousefzadeh, E. Alarcon, D. Maksimovic, "Efficiency optimization in linear assisted switching power converters for envelope tracking in RF power amplifiers", IEEE International Symposium on Circuits and Systems, ISCAS 2005, 23-26 May, pages:1302-1305 Vol. 2
- [14] V. Pinon, F. Hasbani, A. Giry, D. Pache, C. Gamier, "A Single-Chip WCDMA Envelope Reconstruction LDMOS PA with 130MHz Switched-Mode Power Supply," Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International , vol., no., pp.564-636, 3-7 Feb. 2008
- [15] P.G. Blanken, R. Karadi, H.J. Bergveld, "A 50MHz Bandwidth Multi-Mode PA Supply Modulator for GSM, EDGE and UMTS Application", IEEE Radio Frequency Integrated Circuits Symposium, RFIC 2008, 15-17 June 2008
- [16] L.Marco, E. Alarcon, D. Maksimovic, "Effects of switching power converter nonidealities in Envelope Elimination and Restoration technique", IEEE International Symposium on Circuits and Systems, ISCAS 2006, 21-24 May 2006
- [17] M. Vasić, O. Garcia, J.A. Oliver, P. Alou, J.A. Cobos, "Multilevel Power Supply for High Efficiency RF Amplifiers", Applied Power Electronics Conference, APEC '09
- [18] V. Yousefzadeh, "Digitally Controlled Power Converters for RF Power Amplifiers", PhD Thesis, August 2006.

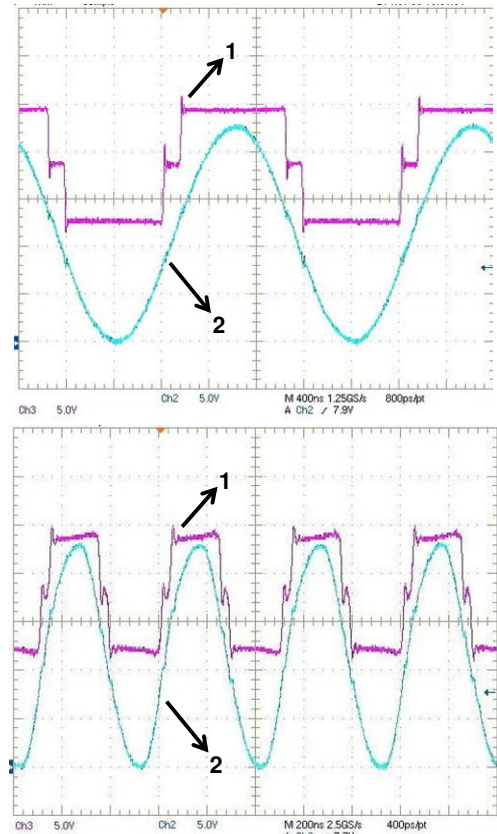


Figure 14. Waveform of multilevel's output voltage (label 1) and linear regulator's output voltage (label 2) at 500 kHz and 2 MHz